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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/933,379	08/20/2001	Ken W. Marr	2008.000282	7000
23720 7590 07/05/2007 WILLIAMS, MORGAN & AMERSON 10333 RICHMOND, SUITE 1100 HOUSTON, TX 77042			EXAMINER FARAHANI, DANA	
			ART UNIT 2891	PAPER NUMBER
			MAIL DATE 07/05/2007	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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Office Action Summary

Application No.

09/933,379

Applicant(s)

MARR, KEN W.

Examiner

Dana Farahani

Art Unit

2891

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 22 December 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 36, 37, 41-43, 45, 46, 50-52 and 54 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 36, 37, 41-43, 45, 46, 50-52 and 54 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 36, 37, 41-43, 45, 46, 50-52 and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Duvvury et al., hereinafter Duvvury (US Patent 6,140,683).

Re. claim 36, Duvvury discloses forming a second doped well 18 within the first doped region, wherein forming the second doped plug includes forming the second doped plug in the second doped well a second distance from a boundary of the second n-well. The second distance is selected, which leads to a particular resistance value. Although, it is not explicitly disclosed that a desired resistance of a current path between the first doped plug and the second doped plug, it is clear that the value of the resistor 30 is left adjustable (see, for example, col. 4, lines 18-24). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to make the adjustment of the second distance, compare figure 2a and 2b, for achieving a certain resistance value to allow for a desired turn on time of the device. The value of resistor 30 would change by changing the second distance because the value of the resistor between region 22 and the well 18 changes, which in turn causes the value of the resistor 30 change.

Re. claims 37, 42, 43, 46, Duvvury discloses a method comprising providing a first p doped region 14;

forming a first n doped well 16 within the first doped region;

selecting a first distance; distance A, plus the distance between A and region 20, to from a first n doped plug 20 to a first boundary of the first doped well to provide approximately a desired breakover voltage between the first doped plug and the first doped region;

forming the first doped plug within the first doped well, wherein the first doped plug is formed the first distance from the first boundary of the first doped well;

forming a second doped n plug 32 into the first doped region; and

forming at least an oxide 24 between the first and second doped plugs.

Although, the reference does not expressly disclose the oxide is LOCOS oxide, it would have been obvious to one of ordinary skill in the art at the time of the invention to use LOCOS oxide, since it is well known in the art that the LOCOS oxide method is the most common surface oxide formation method in semiconductor devices, and it is easy and cheap to do.

Re. claims 41 and 50, a conductor layer, the conductive contacts on top of 20 and 32, is above at least a portion of the first and second doped plugs.

Re. claim 46, Duvvury discloses the limitations in the claim, as discussed above.

Moreover, 12 and 14 comprise a p substrate.

Re. claim 51, Duvvury discloses the claimed limitations, as discussed above, further discloses in an ESD event the voltage of the drain increases (col. 4, lines 35 and 36), implying that a pad is connected to the drain/first doped plug. Also, it discloses the second doped plug, in this case 22, to a voltage source, i.e., ground, as can be seen in the figure. An integrated circuit component, that is gate 28, is on the substrate and connected to the bond pad (see figure 3).

Re. claim 52, a second doped well 18 is within the first doped region, and the second doped plug is in that well.

Re. claim 53, the integrated circuit component comprises an anti-fuse network, by means of the gate and a lateral BJT of the device being turned on during an ESD event, hence a conducting state, which make the gate and the BJT an anti-fuse, by definition.


Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dana Farahani whose telephone number is (571)272-1706. The examiner can normally be reached on M-F 9:00AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on (571)272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DF



B. WILLIAM BAUMEISTER
SUPERVISORY PATENT EXAMINER